UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/738,485	12/15/2000	Peter Korger	99-339	1597

24319 7590 10/17/2005

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/738,485	KORGER, PETER	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *8,9 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 8/1/2005.

Non-Compliance

3. Applicant's amendment filed on August 1, 2005, fails to comply with revised 37 CFR 1.121, which is required as of July 30, 2003. More specifically, applicant uses an incorrect status identifier ("Previously Presented") for amended claim 16. Furthermore, applicant has underlined the period in claim 2 (indicating the addition of a period), even though a period already exists in that claim. In the future, it is asked that applicant review all amendments in order to avoid receiving a notice of non-compliance.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features of claim 19 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet,

even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 15 is objected to because of the following informalities: In the last paragraph, please replace "means for present" with --means for presenting--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 19 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the

specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. More specifically, in claim 19, applicant claims that register states are transferred from a first memory to a second memory prior to said comparing, where, in claim 10, the comparing is the comparing of register states to the register address signal to present a gating signal. However, applicant has not enabled both transferring to a second memory and comparing. Instead, applicant has disclosed one embodiment for comparing (Fig.4) and one embodiment for transferring to a second memory (Fig.5), but no comparison takes place in the latter. And, it is not clear why a comparison would need to be made if the second memory storing the states is to merely be addressed by the register address signal.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 15 recites the limitation "said means for storing" in the last paragraph. There is insufficient antecedent basis for this limitation in the claim because applicant previously mentions "means for storing a plurality of register states" and "means for storing a segment count." For purposes of this examination, the examiner will assume that applicant is referring back to the means for storing a plurality of register states.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-3, 5-7, 10-11, 13-16, 18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Watson, U.S. Patent No. 5,655,132.

13. Referring to claim 1, Watson has taught has taught a circuit comprising:

a) a register stack configured as:

(i) a plurality of segments addressable through a segment address signal. See Fig.4, Fig.5, and Fig.9, for instance, and note that the stack is divided into segments. In general, register addresses ("a") are determined by adding a segment base ("RFG", for instance) and a register offset ("i"). See column 6, line 64, to column 7, line 4. The register address is also a segment address signal because when accessing a particular register, its corresponding segment is also accessed.

(ii) a plurality of registers within each of said plurality of segments, said plurality of registers being addressable through a register address signal. See Fig.9 and note that each segment, in this example, has 32 registers per segment. In addition, registers are accessed through the use of a segment base address (register address signal). See column 6, line 64, to column 7, line 4. Note that the base (RFG, for instance) is used to address a register, and therefore, it is a register address signal.

b) a control circuit connected to said register stack and configured to:

(i) store a plurality of register states. See column 12, lines 32-45 and note that a plurality of states may be stored in a status register. A first state may be a user state (represented by 0, for instance), while a second state would be a supervisor state (represented by 1, for instance).

(ii) store a segment count signal. See the abstract and note that each instruction which is to access a register includes a relative address field. The relative address specifies which register in the segment, relative to the base, will be accessed. This is a segment count signal because the system will count X registers up from the base in order to determine which register to access.

(iii) present said segment address signal responsive to said register states, said segment count signal, and said register address signal. See column 7, line 66, to column 8, line 9, and column 12, lines 32-45, and Fig.9, and note that when accessing local registers, the register states will determine the mode (supervisor/user). Depending on the mode, the appropriate segment base address (register address signal) is determined. Once the segment base address is known, a segment count signal (relative address) is added to it to determine the segment address signal (final register address). Therefore, as can be seen, presenting the segment address signal is responsive to each of the aforementioned items.

c) a state register connected to said control circuit and configured to present said register states to said control circuit, wherein each of said register states has one associated register of said registers. See column 12, lines 32-45, and note that a status register exists. The status register presents a bit indicative of either user state or supervisor state. Each state has one associated register of the stack registers. More specifically, the user state is associated with the local user

registers in the stack while the supervisor state is associated with the supervisor local registers in the stack.

14. Referring to claim 2, Watson has taught a circuit as described in claim 1. Watson has further taught that at least one of said register states is fixed in a global state indicating that data cannot be pushed onto said one associated register. See column 12, lines 32-35, and note global registers in the figures. Also, see column 7, lines 10-16, and note that registers in a global state are fixed registers that cannot be modified. Consequently, a register in the global state cannot have data pushed onto it.

15. Referring to claim 3, Watson has taught a circuit as described in claim 1. Watson has further taught that at least one of said register states is fixed in a stackable state indicating that data can be pushed onto said one associated register. See column 8, lines 52-60, and column 7, lines 20-23, and note that when a register is in the local state, data may be pushed onto the register (i.e., so that it may hold an operand).

16. Referring to claim 5, Watson has taught a circuit as described in claim 1. Watson has further taught that the control circuit comprises a status circuit configured to present a gating signal responsive to both said register address signal and said register states. Looking at column 12, lines 32-45, a state is determined and a base corresponding to the state is determined. For instance, if the state is determined to be a local user state, then the RFBU would be used as a base for register address calculation. Once it is determined what type of register is to be accessed, a signal is inherently sent which will choose the appropriate base address to select. For instance, when in local user mode a signal will select the RFBU as the base address whereas in

the local supervisor mode, the signal will select the RFBS as he base address. The signal which selects the base address is considered the gating signal.

17. Referring to claim 6, Watson has taught a circuit as described in claim 5. Watson has further taught that the status circuit comprises a comparator configured to present said gating signal by comparing said register states and said register address signal. As previously described, each register address corresponds to a register in a particular state (global, local user, local supervisor). The register address is compared to a state (i.e., for the address, the state is determined), and consequently, a gating signal is presented to select a base address.

18. Referring to claim 7, Watson has taught a circuit as described in claim 5. Watson has further taught that said status circuit comprises a memory device configured to store said plurality of register states and present said gating signal responsive to said plurality of register states and said register address signal. See column 12, lines 32-45, and note that the status bit representing supervisor/user mode, which is stored in a memory device (status register) is inherently compared to determine what mode the system is in. For instance, the system knows that if the bit is 1, then the system is in user mode, however, if the bit is 0, then the system is in supervisor mode. These are comparisons to 0 and 1 values. In addition, once the mode is known, the appropriate register address signal (base address) is determined. Then in response to the base address, a gating signal (add signal) is given and a final address may be calculated. Therefore, presenting the gating signal is responsive to the register states and register address signal.

19. Referring to claim 10, Watson has taught a method of controlling a register stack comprising the steps of:

a) comparing a register address with a plurality of register states to present a gating signal. See column 12, lines 32-45, and claim 1, and note that the relative offset is compared to see if it corresponds to a global register, a local user register, or a local supervisor register. Once it is determined what type of register is to be accessed, a signal is inherently sent which will choose the appropriate base address to select. For instance, when in local user mode a signal will select the RFBU as the base address whereas in the local supervisor mode, the signal will select the RFBS as he base address. The signal which selects the base address is considered the gating signal.

b) gating a segment count with said gating signal to present a segment address. As described in part (a), the gating signal is used to gate/select a value from the base value registers and whichever value is selected is then presented as a segment address. So, before the base is selected in response to the gating signal, the base is a segment count (i.e., it is an address count of where the corresponding segment begins). After one of the bases is actually selected by the gating signal, that value is presented as a segment address (i.e., the address of the segment to be accessed). This value would then be sent to an adder to be added to a relative address.

c) addressing a plurality of segments within said register stack with said segment address. From column 7, line 4, it can be seen that the final address is equal to the base (segment address) plus the offset (register address). Therefore, a particular segment among the group of segments is determined by the segment base address.

d) addressing said registers within one of said segments with said register address. See column 7, line 4, and note that the particular register within the segment that is to be accessed is

determined by the relative offset "i". By adding the offset to the segment base, the register associated with that offset in that segment will be accessed.

20. Referring to claim 11, Watson has taught a method as described in claim 10. Watson has further taught that step (a) further comprises the substeps of:

a) presenting a signal communicating said plurality of register states. Clearly, when the state is determined (global, local user, or local supervisor), a signal would inherently be used to specify it. This signal, more specifically, is used to select the segment base address corresponding to the determined state. Otherwise, determining the state would serve no purpose.

b) selecting one of said plurality of register states as said gating signal based upon said register address. Based on the state, different base addresses are used in the calculation of a final address. For instance, if a first relative address is determined to be of a global type, then this determination will result in selecting a global base address for addition. However, if a second relative address is determined to be of a local user type, then this determination will result in selecting a local user base address for addition. Therefore, the state acts as a gating signal.

21. Referring to claim 13, Watson has taught a method as described in claim 10. Watson has further taught the step of incrementing said segment address in response to a push instruction. See Fig.8, column 1, lines 35-44, and column 11, line 65, to column 12, line 18, and note that as each new task is encountered, it gets a new portion of the register stack allocated to it, with a segment base address that is larger than the previous segments address. Therefore, in response to a push (adding information to the stack), the segment address is incremented.

22. Referring to claim 14, Watson has taught a method as described in claim 13. Watson has further taught the step of decrementing said segment address in response to a pop instruction.

See Fig.8, column 1, lines 35-44, and column 11, line 65, to column 12, line 18, and note that as each new task is encountered, it gets a new portion of the register stack allocated to it, with a segment base address that is larger than the previous segments address. On the other hand, when tasks are finished, its register space is deallocated and the previous segments address is reloaded such that it specifies the current segment. This reloading in effect decrements the segment address. Therefore, in response to a pop (removing information from the stack), the segment address is incremented.

23. Referring to claim 15, Watson has taught a circuit comprising:

a) register stack means configured as:

(i) a plurality of segments addressable through a segment address. See Fig.4, Fig.5, and Fig.9, for instance, and note that the stack is divided into segments. In general, register addresses ("a") are determined by adding a segment base ("RFG", for instance) and a register offset ("i"). See column 6, line 64, to column 7, line 4. The register address is also a segment address because when accessing a particular register, its corresponding segment is also accessed.

(ii) a plurality of registers within each of said plurality of segments, said plurality of registers being addressable through a register address. See Fig.9 and note that each segment, in this example, has 32 registers per segment. In addition, registers are accessed through the use of a segment base address (register address signal). See column 6, line 64, to column 7, line 4. Note that the base (RFG, for instance) is used to address a register, and therefore, it is a register address.

b) means for storing a plurality of register states. See column 12, lines 32-45 and note that a plurality of states may be stored in a status register. A first state may be a user state (represented by 0, for instance), while a second state would be a supervisor state (represented by 1, for instance).

c) means for storing a segment count. See the abstract and note that each instruction which is to access a register includes a relative address field. The relative address specifies which register in the segment, relative to the base, will be accessed. This is a segment count signal because the system will count X registers up from the base in order to determine which register to access.

d) means for presenting said segment address responsive to said register address and said plurality of register states and said segment count. See column 7, line 66, to column 8, line 9, and column 12, lines 32-45, and Fig.9, and note that when accessing local registers, the register states will determine the mode (supervisor/user). Depending on the mode, the appropriate segment base address (register address signal) is determined. Once the segment base address is known, a segment count signal (relative address) is added to it to determine the segment address signal (final register address). Therefore, as can be seen, presenting the segment address signal is responsive to each of the aforementioned items.

e) means for presenting said register states to said means for storing, wherein each of said register states has one associated register of said registers. See column 12, lines 32-45, and note that a status register exists. The status register presents a bit indicative of either user state or supervisor state. Each state has one associated register of the stack registers. More specifically, the user state is associated with the local user registers in the stack while the supervisor state is associated with the supervisor local registers in the stack. Note also that if register states are

stored in a state (or status) register, as is done in Watson, then there must inherently be a means for storing those register states in the status register.

24. Referring to claim 16, Watson has taught a circuit as described in claim 1. Watson has further taught that said control circuit comprises a counter configured to present said segment count signal identifying a current segment of said segments at a logical top of said register stack. As described in the abstract, the instruction's relative address field presents the segment count, i.e., the number of registers away from the base address at which the register to be accessed is located. Therefore, since it provides a count, it is a counter. Also, note from column 12, lines 52-67, that the relative address (segment count) is used to determine which set (segment) of registers is to be accessed. Looking at Fig.4, for instance, if the segment count identifies global segment starting an base n, then the segment at the top of the stack would be identified.

25. Referring to claim 18, Watson has taught a method as described in claim 10. Watson has further taught presenting said segment address as a predetermined address responsive to said gating signal having a global state. From column 12, lines 32-45, it can be seen that an "add global address" signal or "add local address" signal would be provided. If a global base address is to be added to an offset to present a final address, then the global base address is predetermined with respect to the time at which it is added to the offset to form the final address/ That is, the global base address must be known before they are added so that the addition may occur. Therefore, the segment address is predetermined.

26. Referring to claim 20, Watson has taught a method as described in claim 10. Watson has further taught storing said segment count prior to said gating. The segment count (offset/relative

address) is stored within the instruction itself before it is selected and propagated in any fashion. Consequently, the segment count is stored prior to the gating.

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watson, as applied above, in view of Guttag, U.S. Patent No. 4,402,042.

29. Referring to claim 4, Watson has taught a circuit as described in claim 1.

a) Watson has further taught that the register stack comprises a first portion disposed within a processor and configured as at least one segment of said plurality of segments. See Fig.2 and note that Fig.2 represents a processor which includes a register file.

b) Watson has not taught that the register stack comprises a second portion disposed external to said processor and configured as at least one segment of said plurality of segments. However, Guttag has taught a system in which registers may be external to the CPU. See column 4, line 64, to column 5, line 3. As disclosed, this allows for increased programming flexibility and for faster response to interrupts. Of course, as is known, it is also beneficial to have registers on-chip as they may be accessed very quickly by the processor. Therefore, in order to realize both advantages, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Watson such that a portion of the registers are external to the CPU.

30. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watson, as applied above.

31. Referring to claim 12, Watson has taught a circuit as described in claim 10. Watson has not explicitly taught writing said plurality of register states into a register under software control in response to a reset handler operation for a processor executing said software. However, Official Notice is taken that the use of reset handlers is well known and accepted in the art. That is, reset handlers are used to reset/restore the system in some manner. Clearly, if a reset is to occur in Watson, due to an error, or power outage, then before any registers can be accessed, the segment base addresses must be set ahead of time. And, this determines the states. For instance, if the global base is set to address 0, then the global state corresponds to a range of registers starting at address 0. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Watson to include a reset handler for setting the states of the system. Note that all registers are under software control (they are read/written to in response to software).

Allowable Subject Matter

32. Claims 8, 9, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

33. Applicant's arguments filed on August 1, 2005, have been fully considered but they are not persuasive.

34. Applicant argues the novelty/rejection of claim 1 on pages 10-11 of the remarks, in substance that:

> "The "local state" and "user state" argued in the Office Action do not appear to be associated with one of the registers in the register file..."
>
> "Watson appears to be silent regarding a status register being connected to some unidentified control circuit."

35. These arguments are not found persuasive for the following reasons:

a) Regarding the first argument, as described in the modified rejection of claim 1, the status register presents a bit indicative of either user state or supervisor state. Each state has one associated register of the stack registers. More specifically, the user state is associated with the local user registers in the stack while the supervisor state is associated with the supervisor local registers in the stack. If multiple registers are associated with a particular state, then clearly one register is associated with that state.

b) Regarding the second argument, the examiner asserts that everything in the system is coupled/connected in some manner (through wires), even if it isn't a direct connection (although the examiner is not conceding that it is not a direct connection). In this particular example, for a register to be accessed, a segment address must first be known, and in order to determine the segment address, the register state must be known. So, there must be a coupling of components so that information may flow to/from the components in order to achieve the necessary results.

36. Applicant argues the novelty/rejection of claim 10 on pages 11-13 of the remarks, in substance that:

> "Nowhere in the above text, or in any other section does Watson appear to expressly disclose or inherently discuss comparing register states with a register address."
>
> "...Watson appears to be silent regarding both a segment count, a gating signal, and a segment address." In addition, an addition operation is "not a gating operation."
>
> "...Watson appears to contemplate that the register file is addressed only through an absolute address. Watson appears to be silent regarding a segment address."

37. These arguments are not found persuasive for the following reasons:

a) Regarding the first argument, the examiner asserts that the comparison is implied at the very least. As previously stated, from column 12, lines 32-45, note that the relative offset is compared to see if it corresponds to a global register, a local user register, or a local supervisor register. Once it is determined what type of register is to be accessed, a signal is inherently sent which will choose the appropriate base address to select. For instance, when in local user mode a signal will select the RFBU as the base address whereas in the local supervisor mode, the signal will select the RFBS as he base address. For more support, applicant's attention is directed to column 12, lines 52-67. It should be noted that applicant has given no specifics of what the claimed comparing operation includes. And, the specification gives no details as to this operation either. All that can be concluded by the examiner is that for a register address going into the comparator, its state is checked, and based on the state, a signal representing that state is produced. Similarly, in Watson, for a register address, its state is checked (whether it corresponds to a local user/local supervisor/global state), and a signal representing that state is produced (which is then used to select the segment base address).

b) Regarding the second argument, the examiner has tried to clarify the rejection. Essentially, the gating signal is the signal used to select the appropriate segment base address which is then used as an input to an adder. Clearly, if multiple segment addresses are available to choose from, a signal must be provided to select the appropriate base. Also, applicant has not defined a gating signal. The examiner asserts that such a selection signal is a gating signal because the signal acts as a gate for the address. When the signal is active, a gate is opened for the selected base to propagate through the system. When the signal is not active, the gate is closed, thereby preventing the selection of the base.

c) Regarding the third argument, while applicant appears to be correct in saying that a single register is accessed explicitly by an absolute address, the absolute address is made up of a combination of a base address and a relative address. The base address locates the segment base of the segment in which the register is located. And, the relative address locates the register within that segment. Therefore, the segment address is still used to determine the segment.

38. Applicant argues the novelty/rejection of claim 3 on page 14 of the remarks, in substance that:

> "...Watson appears to be silent regarding any of the registers within the register file being fixed as stackable...Watson appears to contemplate that the registers can be designated differently at different times."

39. These arguments are not found persuasive for the following reasons:

a) Even if this is the case that they may be designated differently at different times (which appears to be just one embodiment of the invention), a register that is chosen to be in a stackable state for a window of time is fixed as being stackable at least for that window of time. Applicant

has not claimed that the stackable state is fixed for the entire amount of time that the system is operating (i.e., that a stackable register may never change states).

40. Regarding the claim 2 argument on page 14 of the remarks, the examiner has responded to the argument in the rejection of claim 2 above.

41. Regarding the claim 6 argument on page 15 of the remarks, the examiner has responded to the argument in the rejection of claim 6 above.

42. Regarding the claim 11 argument on page 15 of the remarks, the examiner has responded to the argument in the rejection of claim 11 above. Essentially, the signal is used to select a segment base address, and this signal is required, otherwise the system would not know which address to select.

43. Regarding the claim 4 arguments on pages 16-17, the examiner maintains the rejection because Guttag has taught why it is good to have some registers off-chip (for fast interrupt response). Therefore, it would be obvious to implement such a feature in Watson. Applicant argues that this would slow the machine down but it is not clear how applicant has come to this conclusion when Guttag has specifically stated that having some registers external to the chip benefit interrupt processing. Even if the system were to slow down (which the examiner is not conceding), the benefit of faster interrupt response is still achieved, and for those that desire this characteristic, it would have been obvious to implement it.

44. Regarding the claim 12 argument on pages 17-18, the examiner has responded to the argument in the rejection of claim 12 above. Essentially, the examiner feels that nothing

substantial was added to the claim which makes it patentable. All registers are under software control and all processor execute software (these are the limitations added by applicant).

Conclusion

45. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
October 12, 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100